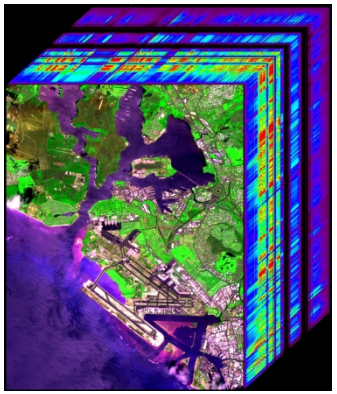
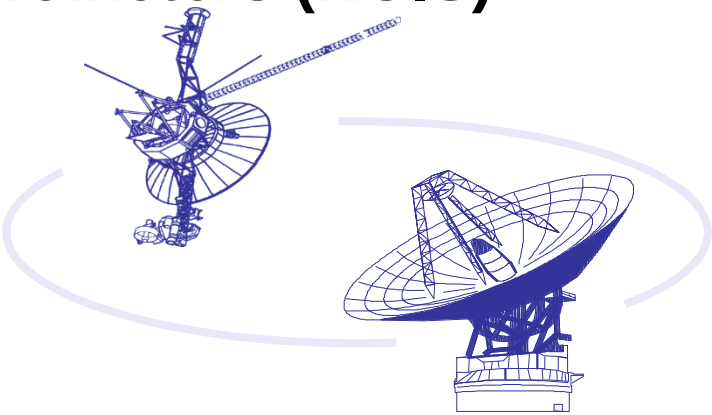
High Performance Space Data Acquisition and Compression with Embedded System-on-Chip Instrument Avionics for Space-based Next Generation Imaging Spectrometers (NGIS)





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Outline

- Overview of Fast Lossless & near-lossless (FL & FLEX) Data Compression for Multispectral Imager (MSI) and Hyperspectral (HSI) imagers
- Data Acquisition and FL & FLEX HW/FW/SW for:
  - Airborne Demonstration
  - Space Deployment

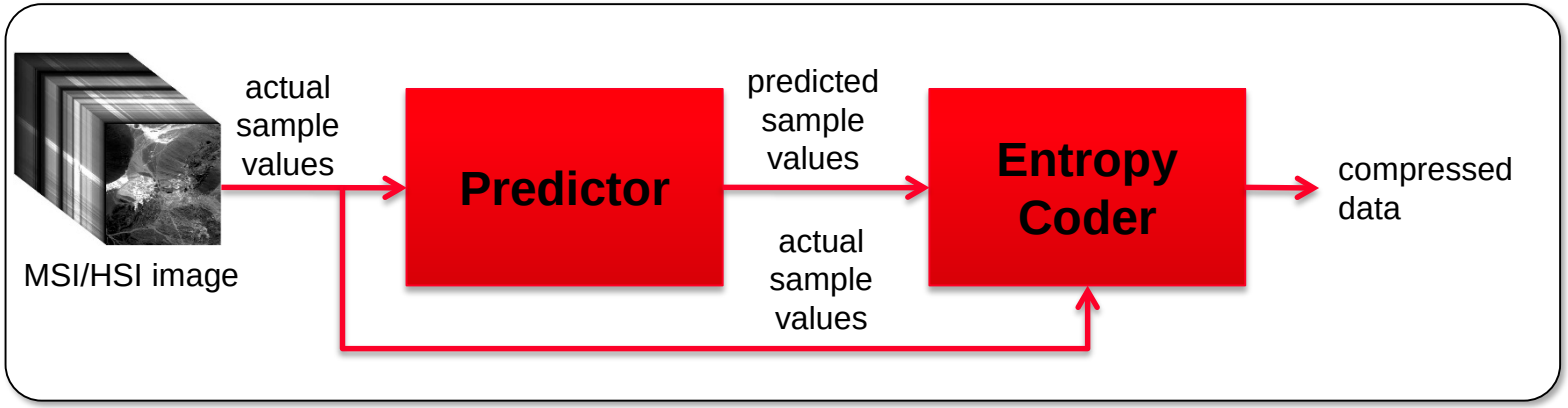
The Need for Compression

- **Imaging spectrometers produce enormous data volumes. A good compressor should:**
  - Exploit spectral dependencies and the 3-dimensional structure of Multispectral Imager (MSI) and Hyperspectral (HSI) to achieve significantly better compression
    - Instead of simply applying 2-dimensional algorithms to each spectral image.
  - Be fast enough for real-time compression as MSI and HSI data are acquired.
    - Modern imaging spectrometers operate at > 10 Msamples/sec (ex: AVIRISng @ 31 Msamples/sec = 62 MBytes/sec)
  - Compress raw, radiance, or reflectance data as needed.
- **Close alignment of AFRL's and NASA's needs for MSI/HSI compression:**
  - High speed compression suitable for real-time onboard implementation
  - Compression specifically tailored to exploit data properties unique to MSI/HSI sensors
  - Maximize data return over constrained communications channels subject to noise and other degradations
  - Maximize utility of delivered data to demanding scientists and other end users

Fast Lossless (FL) MSI/HSI Compressor: Features

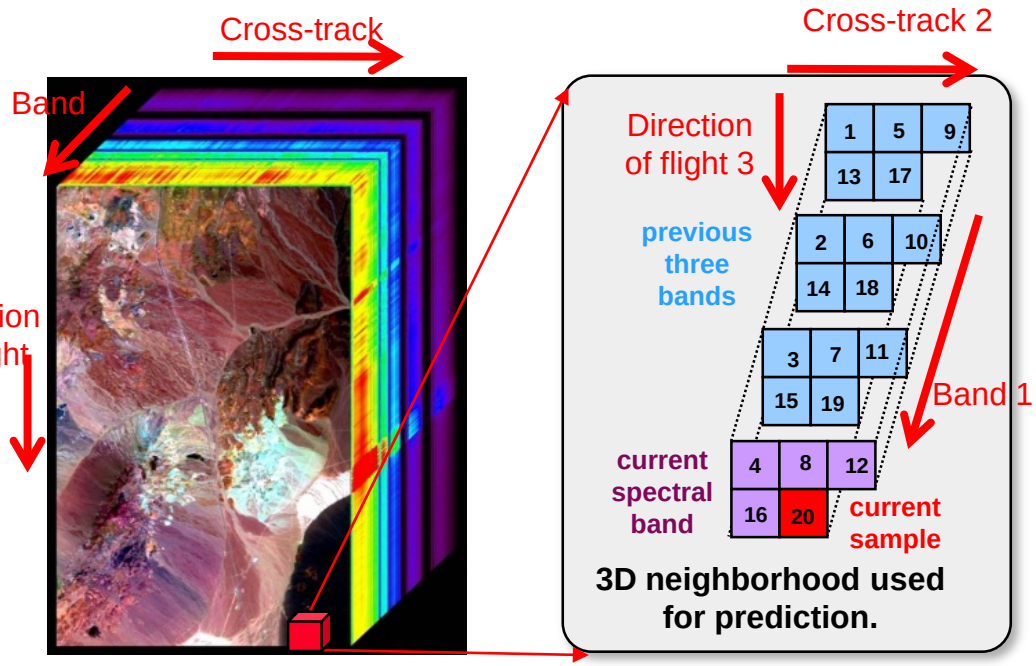
- **Lossless compression** – reconstructed image exactly matches original
- **Excellent compression performance**
- **General purpose**
  - Demonstrated outstanding performance on several different MSI/HSI imaging instruments
    - MaRS, HYCAS, ACES HY, plus CCSDS test set including data from >14 instruments including multispectral imagers, hyperspectral imagers, and ultraspectral sounders
- **Robust** – there is no need to know much in advance about the degree of spectral or spatial correlation
- **Low complexity**
  - Algorithm can be implemented in such a way that the operations per sample are:
    - 6 integer multiplications
    - ~25 integer add, subtract, or bit shift operations
    - entropy coding operations
  - Well-suited for hardware implementation
  - Easily parallelizable
  - Modest memory requirement

Fast Lossless (FL) MSI/HSI Compressor: how it works



Approach: Predictive compression, encoding samples one-at-a-time

- **Predictor**
  - Computes predicted sample value from previously encoded nearby samples (prediction neighborhood illustrated at right)
  - Adaptively adjusts prediction weights for each spectral band via adaptive linear prediction
- **Entropy Coder**
  - Losslessly encodes the *difference between predicted and actual sample values*



Fast Lossless Extended (FLEX): near-lossless MSI/HIS data compressor

- **FLEX achieves *higher compression ratios* than lossless compression and lossy transform-based methods when operating at high-fidelity compression.**
  - FLEX's predictor is specifically tailored to exploit the 3D spectral/spatial structure of HSI data. This distinguishes FLEX from general-purpose image compressors (e.g., JPEG2000, JPEG, JPEG-LS) not designed specifically for HSI data.
- **FLEX's quantizer provides *a quantitative guarantee on the nature of the loss* introduced by compression.**
  - By contrast, transform-based compression approaches (e.g., wavelet-based JPEG2000 or DCT-based JPEG) generally do not control reconstruction error other than in mean square error (MSE) sense. Relevant image features may be locally distorted by an unquantifiable extent.
- **FLEX's implementation approach has substantially *lower complexity* than transform-based compression approaches**
- **Inherits many of the *desirable features of the underlying FL compressor*:**
  - Low computational complexity
  - Single-pass compression & decompression
  - Automatic adaptation to source image data

Example of near-lossless compression performance on a calibrated MaRS hyperspectral image

	File Size	Bit Rate (bits/sample)	Compression
Original image file	385 MB	16	1×
Lossless compression, δ=0	135 MB	5.6	2.9×
Near-lossless, δ=1	96 MB	4.0	4×
Near-lossless, δ=4	67 MB	2.8	5.7×

δ = maximum error in reconstructing the corresponding sample in Data Number

Airborne Demonstration of FLEX Compression

- **Goal:** Airborne In-flight deployment of real-time data calibration and atmospheric correction and FLEX lossless and lossy compression of HSI data over wide operating range.
  - HSI data are acquired by onboard AVIRIS-NG imaging spectrometer, which produces roughly 4 GBytes of raw data per minute during each brief data acquisition period.
  - In-flight data calibration and atmospheric correction (Level 1 and Level 2 data analysis) is performed during data acquisition. Following a given collection period, compression can be performed on one of three data types: raw(L0), calibrated radiance(L1) and calibrated reflectance(L2)
- **COTS Hardware**
  - **Ruggedized COTS PC Hardware (650 Watts):** Supermicro X10DRi motherboard, dual processor Intel Xeon 2.6 GHz (2 each with 14 cores) and eight 32G DDR4, Five Samsung 480GB configured as 1TB RAID 10 with 6Gb/s
  - **Ruggedized COTS Alpha data FPGA Hardware (10 Watts):**
    - Alpha-Data board ADM-XRC-7V1/VX690T-3 with Xilinx Virtex-7 XCV7VX690T-3, Four banks of 2GBytes DDR3 SDRAMs, PCIe x8 Gen2
    - Alpha-Data board ADC-PCIe-XMC designed to carry a single ADM-XMC board
    - Alpha-Data FMC-CLINK-MINI camera link board: transfers HSI image data in real-time (60MBytes/sec) to the Virtex-7
  - **Software/Firmware used for Airborne Deployment**
    - Next Generation Data Collection System (NGDCS) (SW and Firmware)
    - Real-time data analysis (SW) for radiance and reflectance
    - RDUCE FLEX software data compression with and without FPGA (SW and/or Firmware)

SuperMicro PC Hardware

Alpha Data Virtex-7 Board

Alpha Data FMC-CLINK-MINI

AVIRIS-NG HSI Support Equipment

Airborne Demonstration of FLEX: Data Processing Steps

Anatomy of Flight Line

493 Mbits/s (30.7 MSamples/sec) raw instrument data rate (640 cross-track × 481 bands × 16 bits/sample × 100 frames/sec)

500 GBytes average daily of Science data

Step1a & 1b: Data Acquisition & Analysis (radiance and reflectance)

100 sec

Step 2: Compression

6+ min

Reposition aircraft for next flight line

Step1a & 1b: Data Acquisition & Analysis (radiance and reflectance)

time

Data Processing Flow

Step 1a: Acquire L0 data (FPGA)

Operator

PC/FPGA Recording NGDCS

Calibrated BlackBody /Shutter

SSD RAID

Synchronized GPS/IMU data (Level 0)

Raw Instrument Data (Level 0)

Radiance Data (Level 1)

Reflectance Data (Level 2)

Compressed Data

Step 1b: L1/L2 real-time data analysis (PC)

PC Calibration

PC Atmospheric correction

Step 2: Data compression (FPGA/PC)

PC/FPGA FLEX Compression

Flight Compression Experiments (June15 & 16, 2017)

- Flight in Southern California in King Air B200 with AVIRISng.
- Table: Compression options used for each in-flight compression run, with throughput and compression ratios

Typical Data Throughput to compress a 10,000-frame image acquire over 100 sec (including R/W file): AVIRISng 30.7 MSamples/sec

Data Throughput	Raw		Calibrated	
10,000 Frames Image	SW (28 cores)	FPGA (15 cores)	SW (28 cores)	FPGA (15 cores)
File Read/Write (sec) (SW)	16.10	16.00	13.30	13.30
PreProcessing (sec) (SW)	0.40	0.40	22.40	22.40
Compression (sec) (SW/FPGA)	17.40	33.90	14.10	31.80
Total (sec)	33.90	50.30	49.80	67.50
Throughput (MSamples/sec)	**91.26**	**61.51**	**62.12**	**45.83**

Compression Ratio during campaign:

Compression Ratio	Lossless	Lossy δ=9
Raw	3.29	4.70
Radiance	7.19	22.50
Reflectance	4.77	10.39

δ = maximum error in reconstructing the corresponding sample in Data Number

Scene	Input Type	Platform	Custom Profile	Raw Mode?	max_err (in FF units)	SZvault Parity	Elapsed Time (sec)	CPU%	Throughput (Msamples/sec)	Compressed Data Rate (bits/sample)	Compression Ratio
ang20170615t205305	rad	software	none	no	5	0	39.45	2960	79.37	2.39	13.41
ang20170615t212230	rad	software	none	no	0	0	40.59	2888	75.65	4.45	7.19
ang20170615t213955	rad	software	rdn_profile	no	5	0	41.14	2891	75.11	4.17	7.67
ang20170615t221500	rad	software	none	no	21	0	38.85	3010	80.28	0.98	32.51
ang20170615t231426	rad	FPGA	none	no	0	0	414.53	91	7.91	4.49	7.12
ang20170616t175534	rad	software	none	no	2047	0	34.87	3028	88.05	0.03	1036.79
ang20170616t175534	rad	software	none	no	3	3	39.51	2823	77.71	3.00	10.68
ang20170616t175534	rad	software	rfl_profile	no	4	11	45.05	2861	68.16	8.88	3.61
ang20170616t185230	rad	software	rdn_profile	no	97	0	37.27	2939	81.89	1.08	29.55
ang20170616t185230	rad	software	none	yes	9	0	37.24	2986	81.96	1.51	21.15
ang20170616t185230	rad	software	none	no	97	0	35.77	2911	85.32	0.30	105.11
ang20170616t185230	rad	software	none	no	446	0	35.69	2987	85.52	0.08	382.87
ang20170616t185230	rad	software	rdn_profile	no	21	0	38.58	2966	79.11	2.46	13.02
ang20170616t185230	rad	software	rdn_profile	no	4	11	39.93	2848	76.43	4.50	7.11
ang20170616t185230	rad	software	none	yes	1	0	39.18	2881	77.90	4.04	7.91
ang20170616t193255	rad	software	none	no	2047	0	35.9	2925	85.09	0.02	1367.46
ang20170616t193255	rad	software	none	no	3	3	39.33	2863	77.67	3.01	10.64
ang20170616t193255	rad	software	none	no	5	0	38.37	2952	79.61	2.33	13.76
ang20170616t193255	rad	software	none	no	1	0	69.47	1689	43.97	4.48	7.15
ang20170616t193255	rad	FPGA	none	no	1	0	348.39	90	8.77	4.48	7.15
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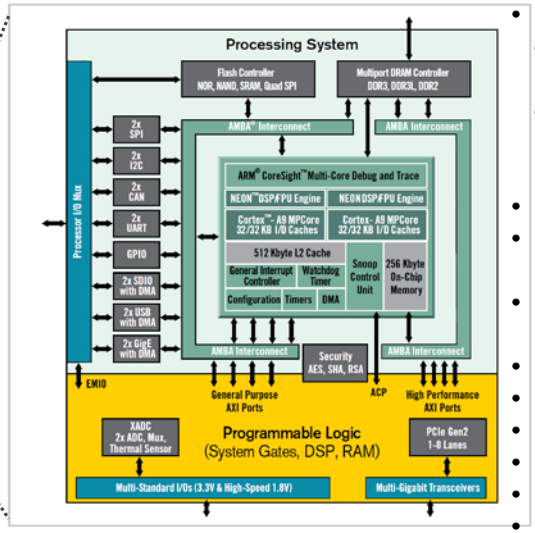
ang20170616t193255	rad	FPGA	none	yes	9	0	333.66	91	9.16	1.42	22.58
ang20170616t193255	rad	FPGA	none	no	21	0	332	91	9.20	0.96	33.41
ang20170615t205305	raw	software	none	yes	0	0	24.68	1981	127.15	4.86	3.29
ang20170615t212230	raw	software	none	no	0	0	27.56	1981	111.66	7.67	2.09
ang20170615t213955	raw	software	none	yes	50	0	21.08	1981	146.91	1.69	9.44
ang20170615t221500	raw	software	none	yes	10	0	23.53	1932	132.83	3.45	4.64
ang20170615t234922	raw	FPGA	none	yes	0	0	122.34	46	68.05	4.70	3.40
ang20170615t231426	raw	software	none	yes	0	0	38.11	1388	86.28	4.78	3.35
ang20170616t175534	raw	software	none	yes	0	16	24.13	1954	127.52	5.13	3.12
ang20170616t193255	raw	software	none	yes	0	8	24.53	1904	124.81	4.89	3.27
ang20170616t193255	raw	software	none	yes	0	16	24.6	1897	124.45	5.06	3.16
ang20170616t193255	raw	software	none	yes	0	0	24.49	1898	125.01	4.74	3.38
ang20170616t193255	raw	FPGA	none	yes	0	0	61.46	49	49.81	4.74	3.38
ang20170616t193255	raw	FPGA	none	yes	10	0	46.58	41	65.72	3.41	4.70
ang20170616t193255	raw	FPGA	none	yes	50	0	45.36	40	67.49	1.65	9.71
ang20170615t205305	rfl	software	none	yes	9	0	40.34	2893	77.62	3.23	9.90
ang20170615t212230	rfl	software	none	no	0	0	42.67	2649	71.97	6.71	4.77
ang20170615t213955	rfl	software	none	no	97	0	37.76	2771	81.84	1.11	28.72
ang20170615t221500	rfl	software	none	no	446	0	37.83	2873	82.44	0.48	66.79
ang20170615t231426	rfl	FPGA	none	no	0	0	324	88	10.13	7.07	4.52
ang20170616t185230	rfl	software	none	no	3	3	42.27	2698	72.20	5.37	5.96
ang20170616t185230	rfl	software	none	no	21	0	38.08	2819	80.15	2.69	11.91
ang20170616t185230	rfl	software	none	yes	1	0	42.18	2579	72.36	6.20	5.16
ang20170616t185230	rfl	software	rfl_profile	no	4	11	43.31	2652	70.47	6.93	4.62
ang20170616t185230	rfl	software	rfl_profile	no	21	0	40.46	2664	75.43	4.47	7.16
ang20170616t185230	rfl	software	none	no	5	0	40.53	2693	75.30	4.59	6.97
ang20170616t185230	rfl	software	rfl_profile	no	5	0	41.03	2668	74.39	6.60	4.85
ang20170616t185230	rfl	software	rfl_profile	no	97	0	37.19	2750	82.07	2.43	13.15
ang20170616t185230	rfl	software	none	no	2047	0	35.23	2822	86.63	0.21	148.93
ang20170616t193255	rfl	software	rfl_profile	no	4	11	43.82	2575	69.71	6.69	4.78
ang20170616t193255	rfl	software	none	yes	9	0	38.73	2725	78.87	3.08	10.39
ang20170616t193255	rfl	FPGA	none	no	5	0	324.43	89	9.42	4.36	7.34

System-on-Chip (SoC) Motivation for Space

COTS SoC FPGA
(e.g. Xilinx Zynq)

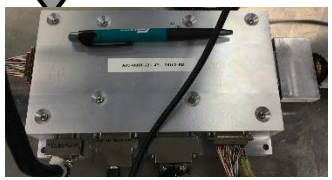


Zynq launched in May 2012, Vendor Zynq board in July 2013

Zynq SoC 7000:

- **Application Processing Unit**:
  - Double Core CORTEX-A9 (Application Profile)
  - Media Processing Engine (SIMD NEON DSP and Floating Point)
- **Programmable Logic**
- **I/O peripherals** (54 multiplexed I/O, 64 Extended I/)
- **Built-in Peripherals** (USB, Ethernet,SPIs,…)
- Memory Interfaces
- PS Interconnects
- DMA
- Timers: Public and Private
- General Interrupt Controller
- On-Chip RAM (OCM)
- Debug Controller
- **VIVADO Design Suite**

SoC FPGA Space technology
(e.g JPL/Alpha Data , NSF CHREC Space Processor)

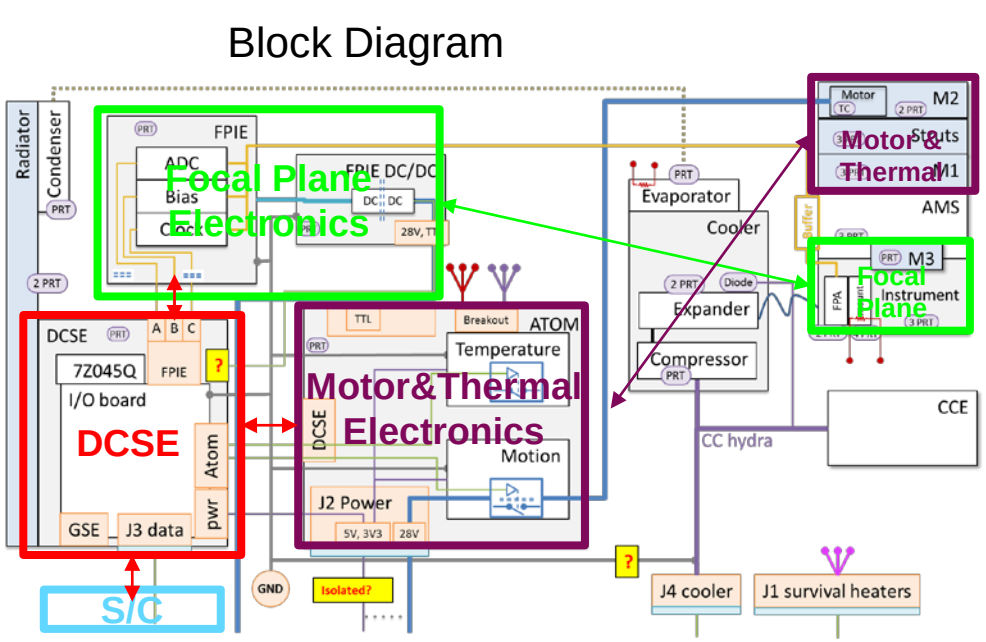


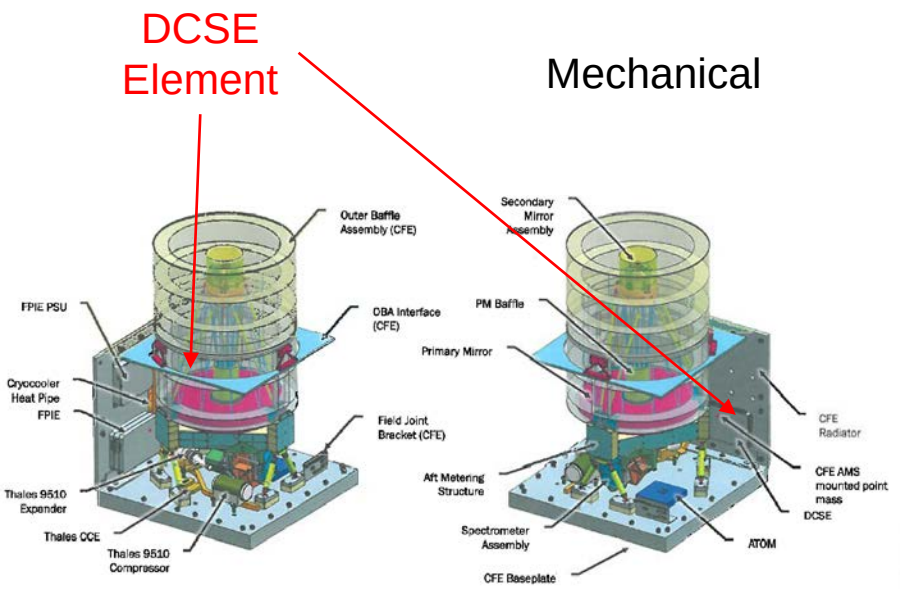
JPL/AlphaData SoC Space Instrument Avionics

Wirthlin et al. " Radiation test within Center for High-Performance Reconfigurable Computing (CHREC) Space Processor (CSP)", MAPLD, May 2015 (pairs Launched on 20 Feb 2017 by SpaceX for ISS for Goddard ISEM experiment)

- For space applications requiring two-chip (CPU and FPGA), System-on-Chip (e.g. Zynq) provides as much as 50% less board space, power and system cost for same Performance and Functionality through:
  - Chip-level integration which eliminates cost of one of the packages and saves board space
  - consolidation external memories between CPU and FPGA to one memory device
  - Internal Communications between the CPU and FPGA consuming substantially less power and offers substantially higher bandwidth and lower latency.
- Aligned with NASA's approach to SoC technology to be used for CubeSats/Small Sat operating in Low Earth Orbit (LEO) and deep-space exploration missions

High Performance Space Data Acquisition and Compression for Next Generation Imaging Spectrometer (NGIS): Capabilities





- The Data Compression and Support Electronics (DCSE) acquires the image from the Focal Plane Interface Electronics (FPIE), losslessly (with lossy capability) compresses with cloud screening the data in real-time, packetizes the compressed data and sends the data to the testbed.
  - DCSE is a hardware board with Zynq Z7045Q which includes Kintex-7 FPGA (*equivalent to 5 rad-hard flight Virtex5 FPGA consuming total of 40 Watts*) and dual-core ARM Cortex-A9 Processors (*equivalent to 10 RAD750 (PowerPC) flight processors consuming total of 50Watts*)
  - Acquires 640×480 samples 16 bits (used 14bits), 125 frames/sec from FPA CHROMA producing at input data rate of 0.5 Gbits/sec
  - Lossless compression and cloud screen in real-time hyperspectral data with a compression ratio of up to 4:1 producing an output compressed data rate of 126 Mbits/sec
  - Program frames rates of FPA CHROMA from 1 MSamples/sec to 40 MSamples/sec. (Nominal is 20 MSamples/sec with 65 frames/sec)
  - Provide housekeeping data with instrument health, safety and timing information
  - Provide digital control of temperature and autofocus mechanism.

Alpha Data modified COTS, FW and SW for NGIS

- **Alpha Data** ALPHA DATA
  - Alpha Data is a leading supplier of high performance Xilinx FPGA based commercial off-the-shelf (COTS) products for embedded system design and deployment.
  - Focusing on the strategic market areas of digital signal processing (DSP), imaging systems, communications, military and aerospace and high performance computing (HPC), Alpha Data has established a global customer base and reputation for leading edge design.
  - Alpha Data offers design services for taking existing COTS products and tailoring them to customers requirements (MCOTS).
    - See www.alpha-data.com for more information.
- **JPL NGIS Spectrometer Project**
  - Zynq hardware alone is not enough; highly ***configurable and complex*** Xilinx chip needs:
    - Customized FPGA design, and Zynq Processor configuration
    - Customized OS, Yocto Linux distribution (instead of bare metal app)
    - Drivers for custom built interface hardware
      - Alpha Data already has well designed ***frameworks*** that allows easy modification and customization, even between different hardware platforms
        - Let's take a look at the modified COTS board and how the high performance data acquisition and compression system works…

DCSE modified COTS Alpha Data Boards and Interface

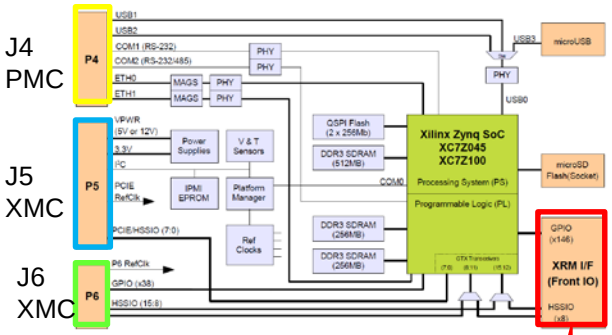
DCSE Hardware:

- Flight modification of COTS Alpha Data ADM-XRC-7Z1/XQ7Z045-2/CC1A Zync SoC XMC Defense Grade
- AlphaData ADC-CUST-&z1 Custom Carrier with buffer, connector, rad hard watch dog timer and Oscillators.
- AlphaData Custom Chassis

DCSE Assembly

Specifications:

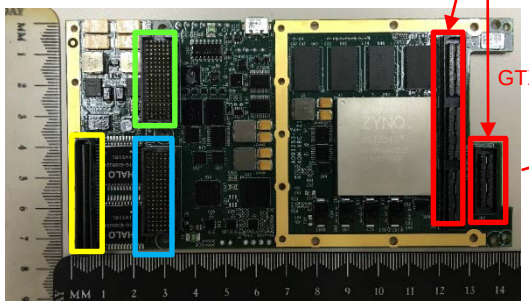
- Volume: 190 by 120 by 30 mm
- Weight: 1Kgr
- Power: 3Watt (ARM); 9 Watt (FPGA+ARM)
- LEO orbit (test COTS parts for destructive Latch-up; eliminate unused functionalities ETH, USB, ucontroller)
- Integrated Rad Hard Parts: oscillator, watch dog timer/hardware reset
- Memories
  - Micron QSPI Flash for Booting (2X256Mbits)
  - Mircron DDR3 SDRAM for PS (512 MBytes) and for PL (2X256 MBytes)
- Interfaces:
  - 146 LVDS for FPIE raw data, compressed data, Full Camera Link (0.5Gbit/sec)
  - SPI (Focal Plane Interface Electronics, ROIC, Heaters, Temperature)
  - RS422 (Cmd & Tlm)



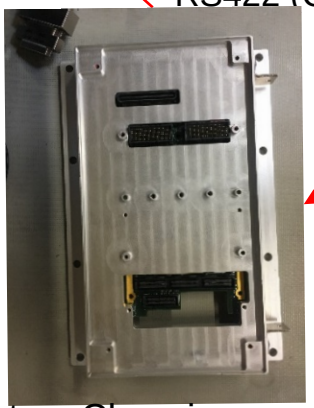
COTS ADM-XRC-7Z1
Block Diagram

GPIO
x146

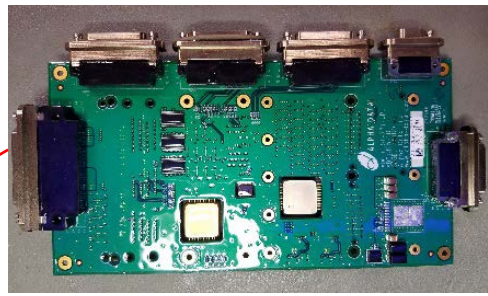
GTX



Alpha Data Modified COTS ADM-XRC-7Z1/XQ7Z045-2/CC1A

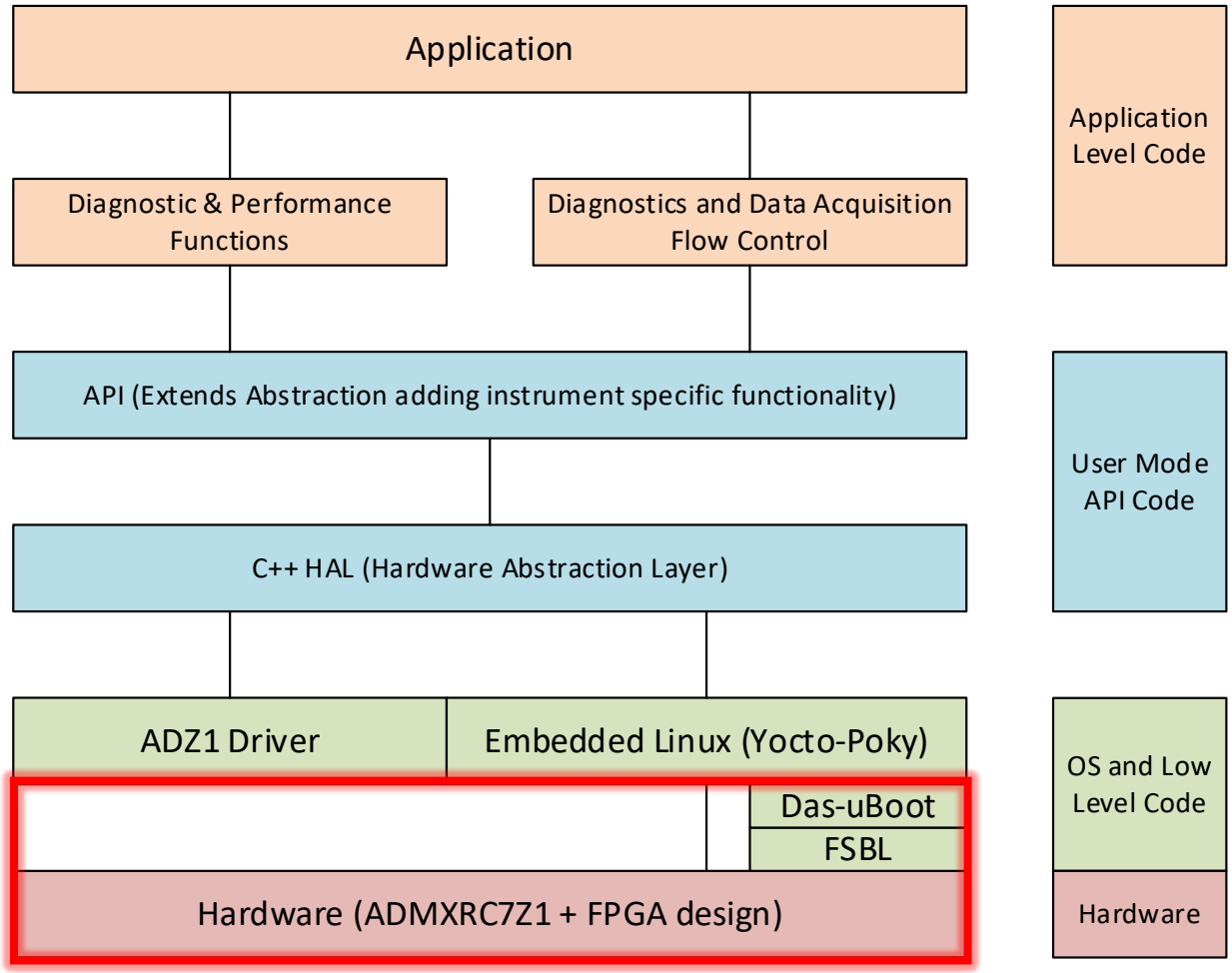


Alpha Data Custom Chassis



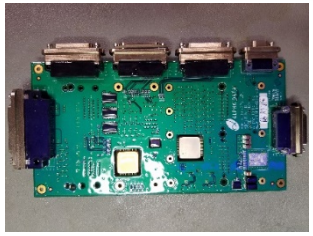
Alpha Data Custom ADC-CUST-7Z1 for external interface

DCSE Bottom Up: Hardware, FPGA Firmware, Boot Procedure



- **Hardware**
  - DCSE starts with COTS CPU/FPGA board ADM-XRC-7Z1 with ADC-CUST-7Z1 carrier board for external interfaces.
  - Build custom high-speed interface board for Focal Plane Interface Electronics, GSE Camera Link, LVDS Data compression output, heaters and motor controller, Commands and telemetry, PPS, GSE diagnostic (COM1,JTAG)
- **FPGA Firmware**
  - Build customized FPGA/ARM architecture with Vivado block diagram editor (based of existing example designs).
  - Add custom VHDL code for application specific needs:
    - Interfacing with Camera Link at 50MHz, LVDS output at 40MHz, LVDS input at 80MHz
    - Data flow control.
    - Hardware data compression
    - Hardware data acquisition.
- **Boot Procedure**
  - First Stage Boot Loader (FSBL) begins on power up
  - FSBL loads u-Boot, which in turn loads Yocto Embedded Linux OS

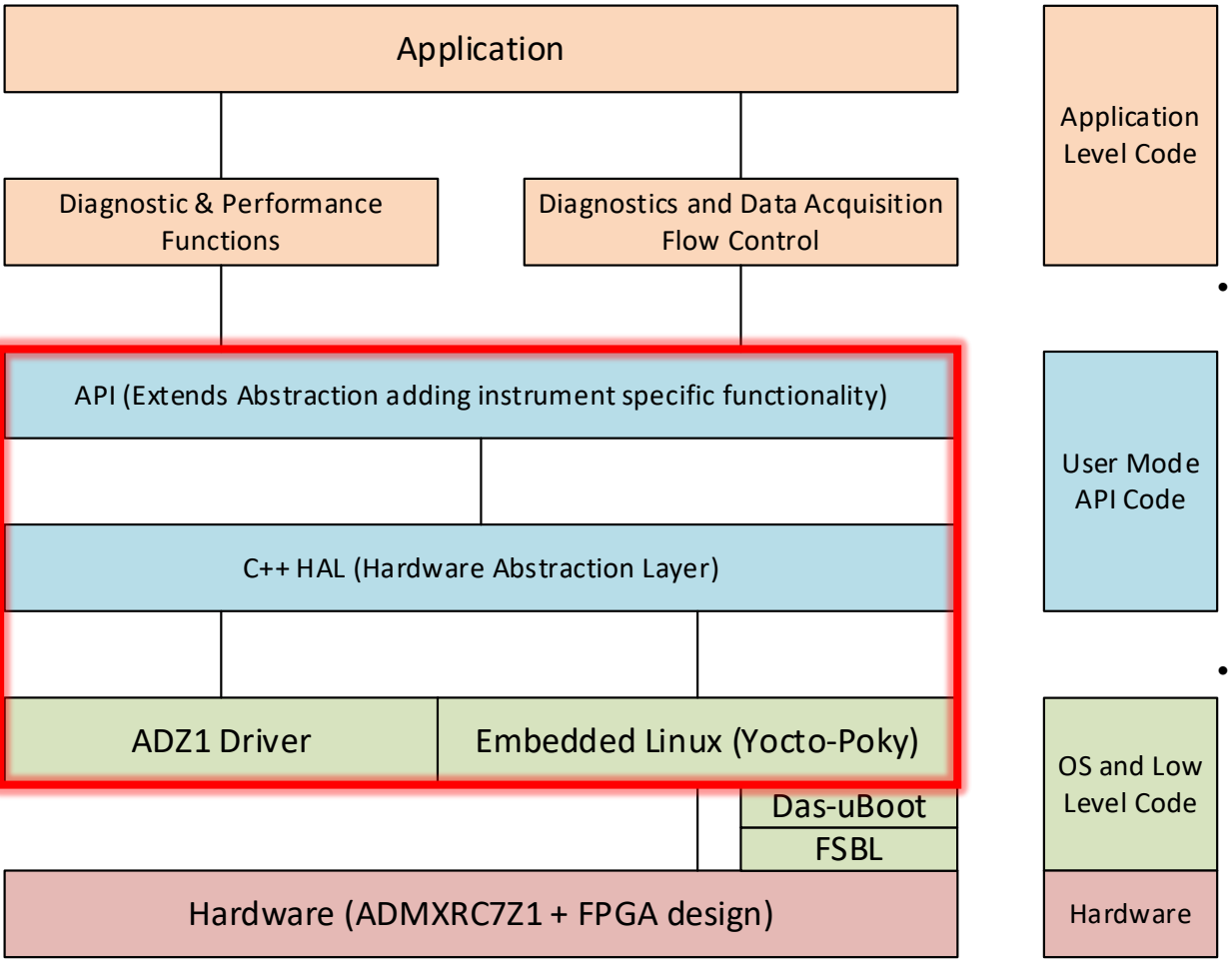
Modified COTS ADM-XRC-7Z1/XQ7Z045-2/CC1A



Custom ADC-CUST-7Z1

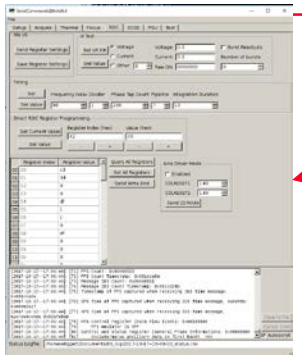
Custom CHASSIS

DCSE Bottom Up: OS, HAL and API

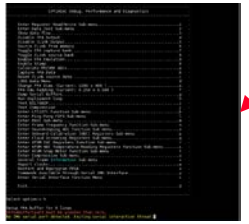


- **Operating System**
  - Customized Yocto Embedded Linux for NGIS project, not just recompiled kernel, but entire distribution contains only necessary components
  - Custom Kernel module (ADZ1) for low level CPU/FPGA interaction (used for interrupts etc)
- **HAL (Hardware Abstraction Layer)**
  - Provides non-application specific functions for interacting with FPGA, and host operating system
  - Allows underlying hardware and/or Operating System to change with minimal impact to project.
  - Lots of ***deployment*** possibilities: other OS, other Alpha Data Cards, or other board vendors
- **API (Application Interface)**
  - DCSE API provides application level interaction with the NGIS sensor(s).
  - Provides initialization and configuration function.
    - DCSE device management: Configuring FPGA
    - ***Fully programmable:*** Image Size, Frame Rate, Focal Plane Array, Compression Parameters and Clouds Screening
  - Provides functions to start/stop data capture
  - Provides functions for house keeping data

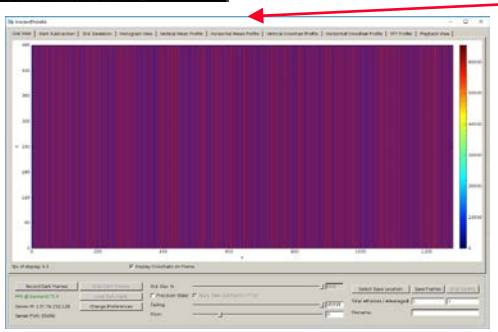
DCSE Bottom Up: Diagnostics, Performance and Applications



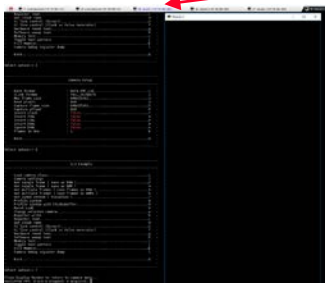
FM Cmd&Tlm
RS422 GUI running on GSE computer



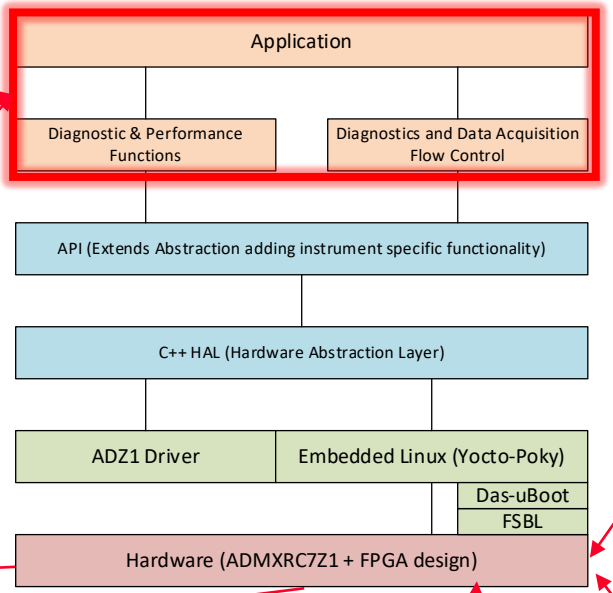
GSE Diagnostics & Performance console mode running on ARM



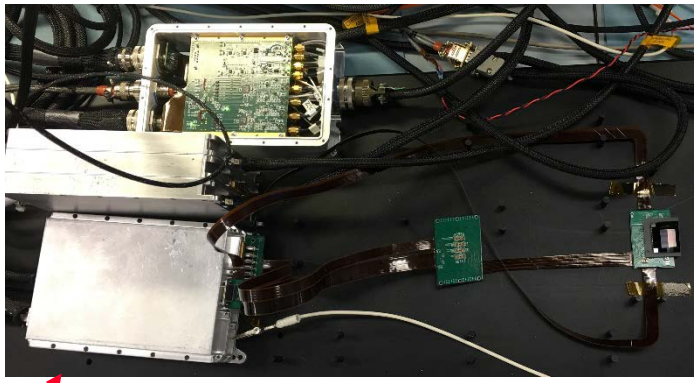
GSE Camera Link uncompressed data grabber running on GSE computer



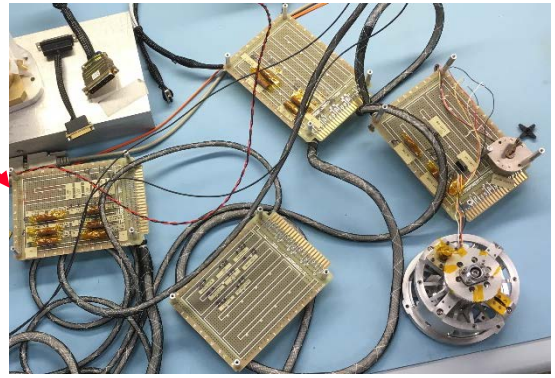
EM LVDS compressed data grabber running on GSE computer



EM Pulse Per Second



EM Focal Plane Interface Electronics & CHROMA

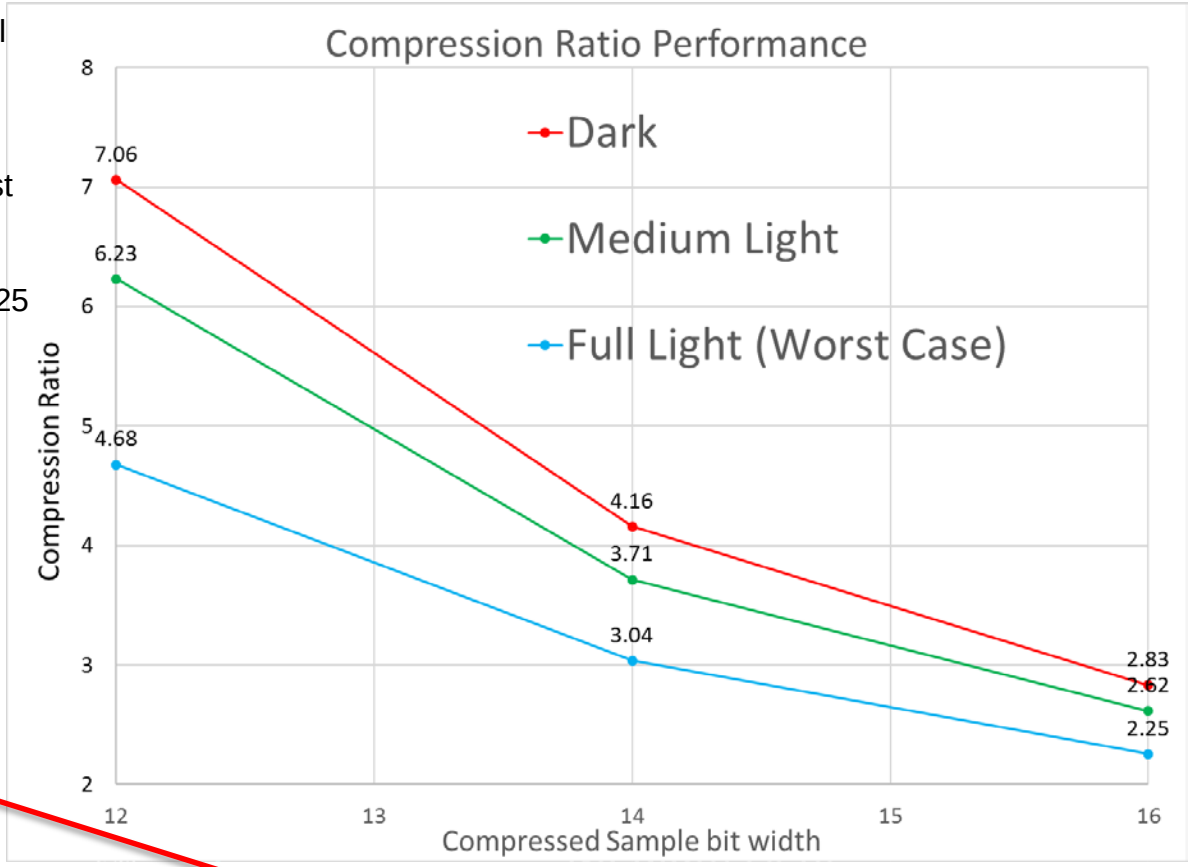


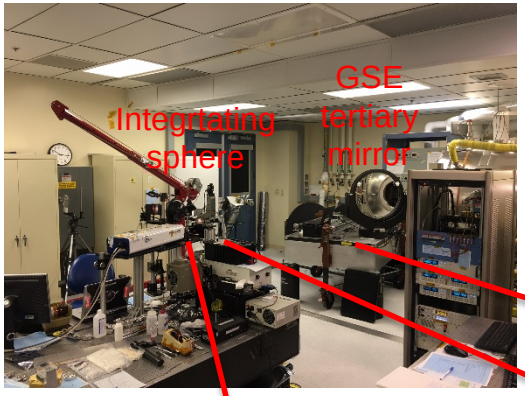
EM 13 Heaters, 1 Step Motor, 32 Temperatures

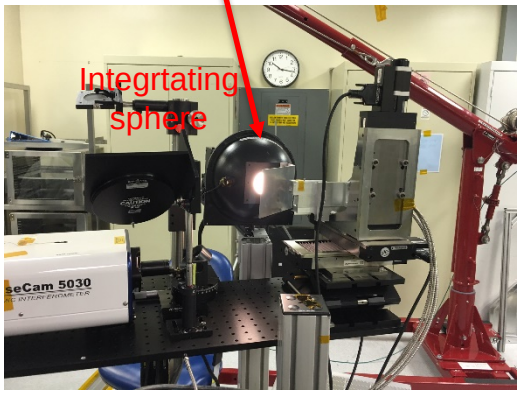
- **Applications**
  - Running multiple threads: data flow control, serial Cmd&Tlm, Motor&Heater
  - Progam camera (CHROMA), focal plane interface electronics (LTC2271), heaters, compression parameters and clouds screening parameters.
  - Control Data Flow: ADC images sample to BIL to BIP transformation to multi core compression to header population to packetisation to LVDS signals
  - Collect Housekeeping data and synchronization with S/C Time message and PPS
  - Handle Cmd&Tlm with S/C
  - Diagnostics to check memory banks, clocks, generate image pattern in FPGA design

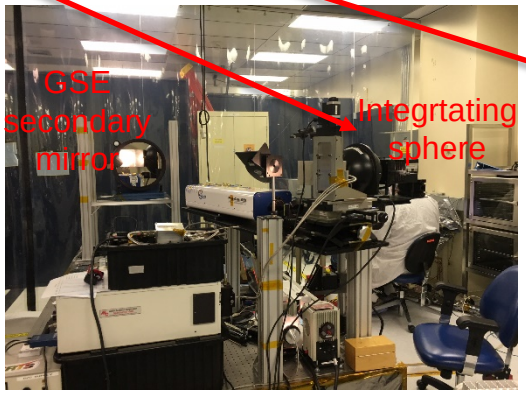
DCSE: Functional and Performance Test

- Used intensively for all optical and thermal control V&V Test of NGIS
- Successfully pass thermal cycle and vibration test.
- Performed functional and performance test at -10°C, 0°C and +15°C in TVAC using Integrating Sphere:
  - Programmable frame rate from 1 to 125 frames/sec
  - Clouds Screening Detection
  - Lossless Compression









Summary

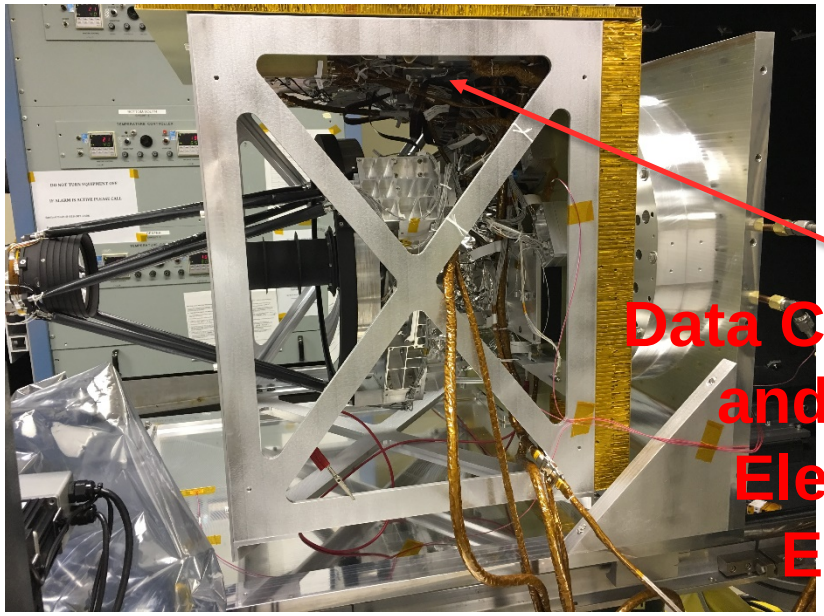
We presented a high performance data acquisition and data compression SW/FW/HW targeting Xilinx Virtex 7 FPGA board for airborne deployment and System-on-Chip (SoC) boards based on modified COTS for space deployment.

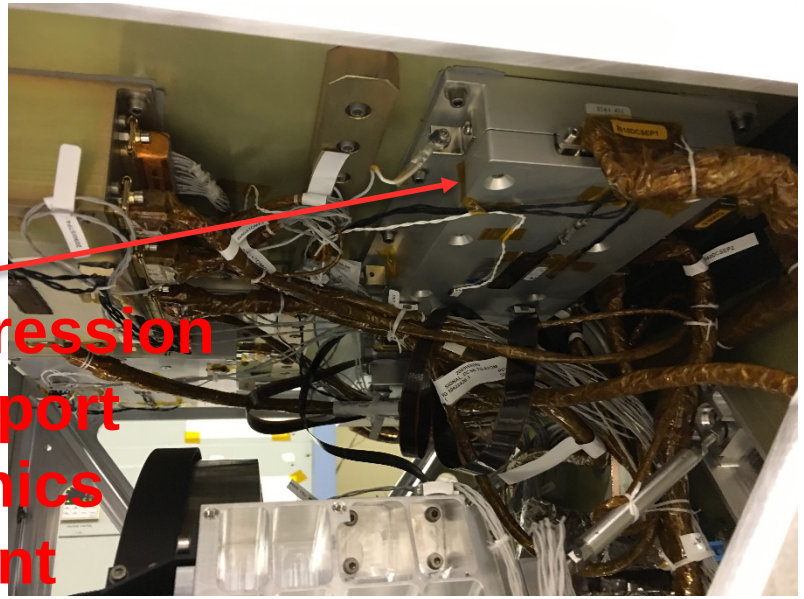
We have integrated single core FLEX data compression targeting Virtex5 FPGA to the ECOSTRESS mission and adapted DCSE data acquisition system for 1280 by 480 frames at 240 frame/sec future HSI instrument.

Future developments will explore new technologies such as Multiple Processor System-on-the-Chip (MPSoC) and space qualified XQR Kintex UltraScale FPGA (XQRKU060) embedded with CHROMA-D which will able to provide hardware resource needed for real-time radiance, reflectance and data analysis.

Back-up
HysplRI 2017 talk

FM DCSE Integrated with NGIS





Data Compression and Support Electronics Element