

High Performance Space Data Acquisition and Compression with Embedded System-on-Chip Instrument Avionics for Space-based Next Generation Imaging Spectrometers (NGIS)





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- Overview of Fast Lossless & near-lossless (FL & FLEX) Data Compression for Multispectral Imager (MSI) and Hyperspectral (HSI) imagers
- Data Acquisition and FL & FLEX HW/FW/SW for:
 - Airborne Demonstration
 - Space Deployment



- Imaging spectrometers produce enormous data volumes. A good compressor should:
 - Exploit spectral dependencies and the 3-dimensional structure of Multispectral Imager (MSI) and Hyperspectral (HSI) to achieve significantly better compression
 - Instead of simply applying 2-dimensional algorithms to each spectral image.
 - Be fast enough for real-time compression as MSI and HSI data are acquired.
 - Modern imaging spectrometers operate at > 10 Msamples/sec (ex: AVIRISng @ 31 Msamples/sec = 62 MBytes/sec)
 - Compress raw, radiance, or reflectance data as needed.

• Close alignment of AFRL's and NASA's needs for MSI/HSI compression:

- High speed compression suitable for real-time onboard implementation
- Compression specifically tailored to exploit data properties unique to MSI/HSI sensors
- Maximize data return over constrained communications channels subject to noise and other degradations
- Maximize utility of delivered data to demanding scientists and other end users



Fast Lossless (FL) MSI/HSI Compressor: Features

- Lossless compression reconstructed image exactly matches original
- Excellent compression performance
- General purpose
 - Demonstrated outstanding performance on several different MSI/HSI imaging instruments
 - MaRS, HYCAS, ACES HY, plus CCSDS test set including data from >14 instruments including multispectral imagers, hyperspectral imagers, and ultraspectral sounders
- Robust there is no need to know much in advance about the degree of spectral or spatial correlation
- Low complexity
 - Algorithm can be implemented in such a way that the operations per sample are:
 - 6 integer multiplications
 - \sim 25 integer add, subtract, or bit shift operations
 - entropy coding operations
 - Well-suited for hardware implementation
 - Easily parallelizable
 - Modest memory requirement



Fast Lossless (FL) MSI/HSI Compressor: how it works



Approach: Predictive compression, encoding samples one-at-a-time

- Predictor
 - Computes predicted sample value from previously encoded nearby samples (prediction neighborhood illustrated at right)
 - Adaptively adjusts prediction of flight weights for each spectral band via adaptive linear prediction
- Entropy Coder
 - Losslessly encodes the difference between predicted and actual sample values





Fast Lossless Extended (FLEX): near-lossless MSI/HIS data compressor

- FLEX achieves higher compression ratios than lossless compression and lossy transform-based methods when operating at high-fidelity compression.
 - FLEX's predictor is specifically tailored to exploit the 3D spectral/spatial structure of HSI data. This distinguishes FLEX from general-purpose image compressors (e.g., JPEG2000, JPEG, JPEG-LS) not designed specifically for HSI data.
- FLEX's quantizer provides a quantitative guarantee on the nature of the loss introduced by compression.
 - By contrast, transform-based compression approaches (e.g., wavelet-based JPEG2000 or DCT-based JPEG) generally do not control reconstruction error other than in mean square error (MSE) sense. Relevant image features may be locally distorted by an unquantifiable extent.
- FLEX's implementation approach has substantially *lower complexity* than transform-based compression approaches
- Inherits many of the desirable features of the underlying FL compressor:
 - Low computational complexity
 - Single-pass compression & decompression
 - Automatic adaptation to source image data

Example of near-lossless compression performance on a calibrated MaRS hyperspectral image

	File Size	Bit Rate (bits/sample)	Compression
Original image file	385 MB	16	1×
Lossless compression, δ=0	135 MB	5.6	2.9×
Near-lossless, δ=1	96 MB	4.0	4×
Near-lossless, δ=4	67 MB	2.8	5.7×

 δ = maximum error in reconstructing the corresponding sample in Data Number 6



Airborne Demonstration of FLEX Compression

- **Goal:** Airborne In-flight deployment of real-time data calibration and atmospheric correction and FLEX lossless and lossy compression of HSI data over wide operating range.
 - HSI data are acquired by onboard AVIRIS-NG imaging spectrometer, which produces roughly 4 GBytes of raw data per minute during each brief data acquisition period.
 - In-flight data calibration and atmospheric correction (Level 1 and Level 2 data analysis) is performed during data acquisition. Following a given collection period, compression can be performed on one of three data types: raw(L0), calibrated radiance(L1) and calibrated reflectance(L2)
- **COTS Hardware**
 - Ruggedized COTS PC Hardware (650 Watts): Supermicro X10DRi motherboard, dual processor Intel Xeon 2.6 GHz (2 each with 14 cores) and eight 32G DDR4, Five Samsung 480GB configured as 1TB RAID 10 with 6Gb/s
 - Ruggedized COTS Alpha data FPGA Hardware (10 Watts):
 - Alpha-Data board ADM-XRC-7V1/VX690T-3 with Xilinx Virtex-7 XCV7VX690T-3, Four banks of 2GBytes DDR3 SDRAMs, PCIe x8 Gen2
 - Alpha-Data board ADC-PCIe-XMC designed to carry a single ADM-XMC board
 - Alpha-Data FMC-CLINK-MINI camera link board: transfers HSI image data in real-time (60MBytes/sec) to the Virtex-7
 - Software/Firmware used for Airborne Deployment
 - Next Generation Data Collection System (NGDCS) (SW and Firmware)
 - Real-time data analysis (SW) for radiance and reflectance
 - RDUCE FLEX software data compression with and without FPGA (SW and/or Firmware)



SuperMicro PC Hardware



Alpha Data Virtex-7 Board



Alpha Data FMC-CLINK-MINI



AVIRIS-NG HSI Support Equipment

Airborne Demonstration of FLEX: Data Processing Steps





Flight Compression Experiments (June15 & 16, 2017)

- Flight in Southern California in King Air B200 with AVIRISng.
- Table: Compression options used for each in-flight compression run, with throughput and compression ratios

ang20170616t193255

FPGA

none



Typical Data Throughput to compress a 10,000frame image acquire over 100 sec (including R/W file): AVIRISng 30.7 MSamples/sec

Data Throughput	Ra	w	Calibrated		
	SW (28	FPGA (15	SW (28	FPGA (15	
10,000 Frames Image	cores)	cores)	cores)	cores)	
File Read/Write (sec) (SW)	16.10	16.00	13.30	13.30	
PreProcessing (sec) (SW)	0.40	0.40	22.40	22.40	
Compression (sec) (SW/FPGA)	17.40	33.90	14.10	31.80	
Total (sec)	33.90	50.30	49.80	67.50	
Throughput (MSamples/sec)	91.26	61.51	62.12	45.83	

Compression Ratio during campaign:

Compression Ratio	Lossless	Lossy
		δ =9
Raw	3.29	4.70
Radiance	7.19	22.50
Reflectance	4.77	10.39

 δ = maximum error in reconstructing the corresponding sample in Data Number

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System-on-Chip (SoC) Motivation for Space



- Zyng board in July 2013
 - For space applications requiring two-chip (CPU and FPGA), System-on-Chip (e.g. Zyng) provides as much as 50% less board space, power and system cost for same Performance and Functionality through:
 - Chip-level integration which eliminates cost of one of the packages and saves board space
 - consolidation external memories between CPU and FPGA to one memory device
 - Internal Communications between the CPU and FPGA consuming substantially less power and offers substantially higher bandwidth and lower latency.
- Aligned with NASA's approach to SoC technology to be used for CubeSats/Small Sat operating in Low Earth Orbit (LEO) and deep-space exploration missions



High Performance Space Data Acquisition and Compression for Next Generation Imaging Spectrometer (NGIS): Capabilities



- The Data Compression and Support Electronics (DCSE) acquires the image from the Focal Plane Interface Electronics (FPIE), losslessly (with lossy capability) compresses with cloud screening the data in real-time, packetizes the compressed data and sends the data to the testbed.
 - DCSE is a hardware board with Zynq Z7045Q which includes Kintex-7 FPGA (equivalent to 5 rad-hard flight Virtex5 FPGA consuming total of 40 Watts) and dual-core ARM Cortex-A9 Processors (equivalent to 10 RAD750 (PowerPC) flight processors consuming total of 50Watts)
 - Acquires 640×480 samples 16 bits (used 14bits), 125 frames/sec from FPA CHROMA producing at input data rate of 0.5 Gbits/sec
 - Lossless compression and cloud screen in real-time hyperspectral data with a compression ratio of up to 4:1 producing an output compressed data rate of 126 Mbits/sec
 - Program frames rates of FPA CHROMA from 1 MSamples/sec to 40 MSamples/sec. (Nominal is 20 MSamples/sec with 65 frames/sec)
 - Provide housekeeping data with instrument health, safety and timing information
 - Provide digital control of temperature and autofocus mechanism.



- Alpha Data 🔗 Alpha data
 - Alpha Data is a leading supplier of high performance Xilinx FPGA based commercial off-the-shelf (COTS) products for embedded system design and deployment.
 - Focusing on the strategic market areas of digital signal processing (DSP), imaging systems, communications, military and aerospace and high performance computing (HPC), Alpha Data has established a global customer base and reputation for leading edge design.
 - Alpha Data offers design services for taking existing COTS products and tailoring them to customers requirements (MCOTS).
 - See <u>www.alpha-data.com</u> for more information.
- JPL NGIS Spectrometer Project
 - Zynq hardware alone is not enough; highly *configurable and complex* Xilinx chip needs:
 - Customized FPGA design, and Zynq Processor configuration
 - Customized OS, Yocto Linux distribution (instead of bare metal app)
 - Drivers for custom built interface hardware
 - Alpha Data already has well designed *frameworks* that allows easy modification and customization, even between different hardware platforms
 - Let's take a look at the modified COTS board and how the high performance data acquisition and compression system works...

DCSE modified COTS Alpha Data Boards and Interface

DCSE Hardware:

- Flight modification of COTS Alpha Data ADM-XRC-7Z1/XQ7Z045-2/CC1A Zync SoC XMC Defense Grade
- AlphaData ADC-CUST-&z1 Custom Carrier with buffer, connector, rad hard watch dog timer and Oscillators.
- AlphaData Custom Chassis





DCSE Assembly

Specifications:

- Volume: 190 by 120 by 30 mm
- Weight: 1Kgr
- Power: 3Watt (ARM); 9 Watt (FPGA+ARM)
- LEO orbit (test COTS parts for destructive Latch-up; eliminate unused functionalities ETH, USB, ucontroller)
- Integrated Rad Hard Parts: oscillator, watch dog timer/hardware reset

Memories

- Micron QSPI Flash for Booting (2X256Mbits)
- Mircron DDR3 SDRAM for PS (512 MBytes) and for PL (2X256 MBytes)

Interfaces:

- 146 LVDS for FPIE raw data, compressed data, Full Camera Link (0.5Gbit/sec)
- SPI (Focal Plane Interface Electronics, ROIC, Heaters, Temperature)
 RS422 (Cmd & Tlm)



Alpha Data Custom Chassis



Alpha Data Custom ADC-CUST-7Z1 for external interface



DCSE Bottom Up: Hardware, FPGA Firmware, Boot Procedure



Modified COTS ADM-XRC-7Z1/XQ7Z045-2/CC1A

Custom ADC-CUST-7Z1

Custom CHASSIS

Hardware

- DCSE starts with COTS CPU/FPGA board ADM-XRC-7Z1 with ADC-CUST-7Z1 carrier board for external interfaces.
- Build custom high-speed interface board for Focal Plane Interface Electronics, GSE Camera Link, LVDS Data compression output, heaters and motor controller, Commands and telemetry, PPS, GSE diagnostic (COM1,JTAG)

• FPGA Firmware

- Build customized FPGA/ARM architecture with Vivado block diagram editor (based of existing example designs).
- Add custom VHDL code for application specific needs:
 - Interfacing with Camera Link at 50MHz, LVDS output at 40MHz, LVDS input at 80MHz
 - Data flow control.
 - Hardware data compression
 - Hardware data acquisition.
- Boot Procedure
 - First Stage Boot Loader (FSBL) begins on power up
 - FSBL loads u-Boot, which in turn loads Yocto Embedded Linux OS



DCSE Bottom Up: OS, HAL and API



- Frame Rate, Focal Plane Array, **Compression Parameters and Clouds Screening**
- Provides functions to start/stop data capture
- Provides functions for house keeping data



DCSE Bottom Up: Diagnostics, Performance and Applications



- Running multiple threads: data flow control, serial Cmd&Tlm, Motor&Heater
- Progam camera (CHROMA), focal plane interface electronics (LTC2271), heaters, compression parameters and clouds screening parameters.
- Control Data Flow: ADC images sample to BIL to BIP transformation to multi core compression to header population to packetisation to LVDS signals
- Collect Housekeeping data and synchronization with S/C Time message and PPS
- Handle Cmd&Tlm with S/C
- Diagnostics to check memory banks, clocks, generate image pattern in FPGA design



DCSE: Functional and Performance Test

- Used intensively for all optical and thermal control V&V Test of NGIS
- Successfully pass thermal cycle and vibration test.
- Performed functional and performance test at -10°C, 0°C and +15°C in TVAC using Integrating Sphere:
 - Programmable frame rate from 1 to 125 frames/sec
 - Clouds Screening Detection
 - Lossless Compression









Summary

We presented a high performance data acquisition and data compression SW/FW/HW targeting Xilinx Virtex 7 FPGA board for airborne deployment and System-on-Chip (SoC) boards based on modified COTS for space deployment.

We have integrated single core FLEX data compression targeting Virtex5 FPGA to the ECOSTRESS mission and adapted DCSE data acquisition system for 1280 by 480 frames at 240 frame/sec future HSI instrument.

Future developments will explore new technologies such as Multiple Processor System-on-the-Chip (MPSoC) and space qualified XQR Kintex UltraScale FPGA (XQRKU060) embedded with CHROMA-D which will able to provide hardware resource needed for real-time radiance, reflectance and data analysis.



Back-up HyspIRI 2017 talk



FM DCSE Integrated with NGIS





